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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,643	12/01/2004	Fabrizio Campanale	CH 020020	8779

65913 7590 02/07/2008

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EXAMINER	
RABOVIANSKI, ANTON I	
ART UNIT	**PAPER NUMBER**
2188	

NOTIFICATION DATE	DELIVERY MODE
02/07/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/516,643	CAMPANALE, FABRIZIO	
	Examiner	Art Unit	
	Anton Rabovianski	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/15/2007 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-8 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai *et al.* (US 5,974,528) in view of Hertwig *et al.* (US 2002/0049888).

With respect to claim 1, the Tsai *et al.* reference teaches a method for writing data from a processor (fig. 3, el. 310) to a non-volatile memory embedded in an integrated circuit (fig. 3, el. 330), comprising the following steps: (a) at least part of said data to be written to said non-volatile memory is transferred to a volatile memory (col. 8, lines 37-47), (b) when the part of said data has been transferred to said volatile memory, a wait signal is sent to said processor (col. 8, lines 48-50), (c) said part of said

data is transferred from said volatile memory to said non-volatile memory (col. 8, lines 50-59), (d) said wait signal is removed (col. 8, lines 59-65). Tsai *et al.* do not disclose an interface circuit that intercepts the access of the processor to the non-volatile memory for writing data to the non-volatile memory, sending a wait signal and removing it to the processor and transferring the data from the volatile to the non-volatile memory. Hertwig *et al.* disclose an interface circuit (fig. 1, el. 7 and 8) that intercepts the access of the processor to the non-volatile memory for writing data to the non-volatile memory (page 3, [0030]), sending a wait signal and removing it to the processor (page 3, [0032], i.e. interrupt signal) and transferring the data from the volatile to the non-volatile memory (page 3, [0032]). Since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as shown by Tsai *et al.* modified by Hertwig *et al.* with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

With respect to claim 3, Tsai *et al.* further disclose at the beginning of the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in write mode (col. 8, lines 37-62).

Regarding claim 4, Tsai *et al.* further disclose during the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in program mode (col. 8, lines 37-62).

Regarding claim 5, Tsai *et al.* further disclose at the end of the data transfer from the volatile memory to the non-volatile memory, said non-volatile memory is set in read mode (col. 8, lines 37-62).

Regarding claim 6, Tsai *et al.* further teach all of the data is transferred first to the volatile memory (col. 8, lines 37-47).

With respect to claim 7, Tsai *et al.* further disclose the addresses corresponding to the data to be written to the non-volatile memory are stored intermediately (col. 7, lines 41-48).

Regarding claim 8, Tsai *et al.* further teach before the data is written to the volatile memory, the wait signal is sent to the processor and is removed after said data is completely written to said volatile memory (col. 7, lines 49-67 and col. 8, lines 48-65).

Regarding claim 10, Tsai *et al.* further teach the non-volatile memory is a flash memory (col. 7, lines 41-44).

With respect to claim 11, the Tsai *et al.* reference does not disclose the volatile memory is a random access memory or a static random access memory. Hertwig *et al.* disclose random access memory (fig. 1, el. 9). Since random access memory was known in the prior art and one skilled in the art could have combined the elements as shown by Tsai *et al.* modified by Hertwig *et al.* with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Regarding claim 12, Tsai *et al.* further disclose the volatile memory is an embedded volatile memory (fig. 3, el. 340).

Regarding claim 13, Tsai *et al.* disclose an integrated circuit (fig. 3) comprising: a processor (fig. 3, el. 310); a non-volatile memory embedded in the integrated circuit and coupled to said processor (fig. 3, el. 330) and the following steps: (a) at least part of said data to be written to said non-volatile memory is transferred to a volatile memory (col. 8, lines 37-47), (b) when the part of said data has been transferred to said volatile memory, a wait signal is sent to said processor (col. 8, lines 48-50), (c) said part of said data is transferred from said volatile memory to said non-volatile memory (col. 8, lines 50-59), (d) said wait signal is removed (col. 8, lines 59-65). Tsai *et al.* do not disclose an interface circuit coupled to the processor and to the non-volatile memory that intercepts the access of the processor to the non-volatile memory for writing data to the non-volatile memory, sending a wait signal and removing it to the processor and transferring the data from the volatile to the non-volatile memory. Hertwig *et al.* disclose an interface circuit coupled to the processor and to the non-volatile memory (fig. 1, el. 7 and 8) that intercepts the access of the processor to the non-volatile memory for writing data to the non-volatile memory (page 3, [0030]), sending a wait signal and removing it to the processor (page 3, [0032], i.e. interrupt signal) and transferring the data from the volatile to the non-volatile memory (page 3, [0032]). Since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as shown by Tsai *et al.* modified by Hertwig *et al.* with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-8 and 9-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anton Rabovianski whose telephone number is 571-270-1026. The examiner can normally be reached on M-Th 9:00am-7:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR

Anton Rabovianski

January 29, 2008

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
02/01/08